Penn Trigger Board

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Penn Trigger Board

Developed and run for 35 t DUNE prototype to solve nearly identical problem as protoDUNE:

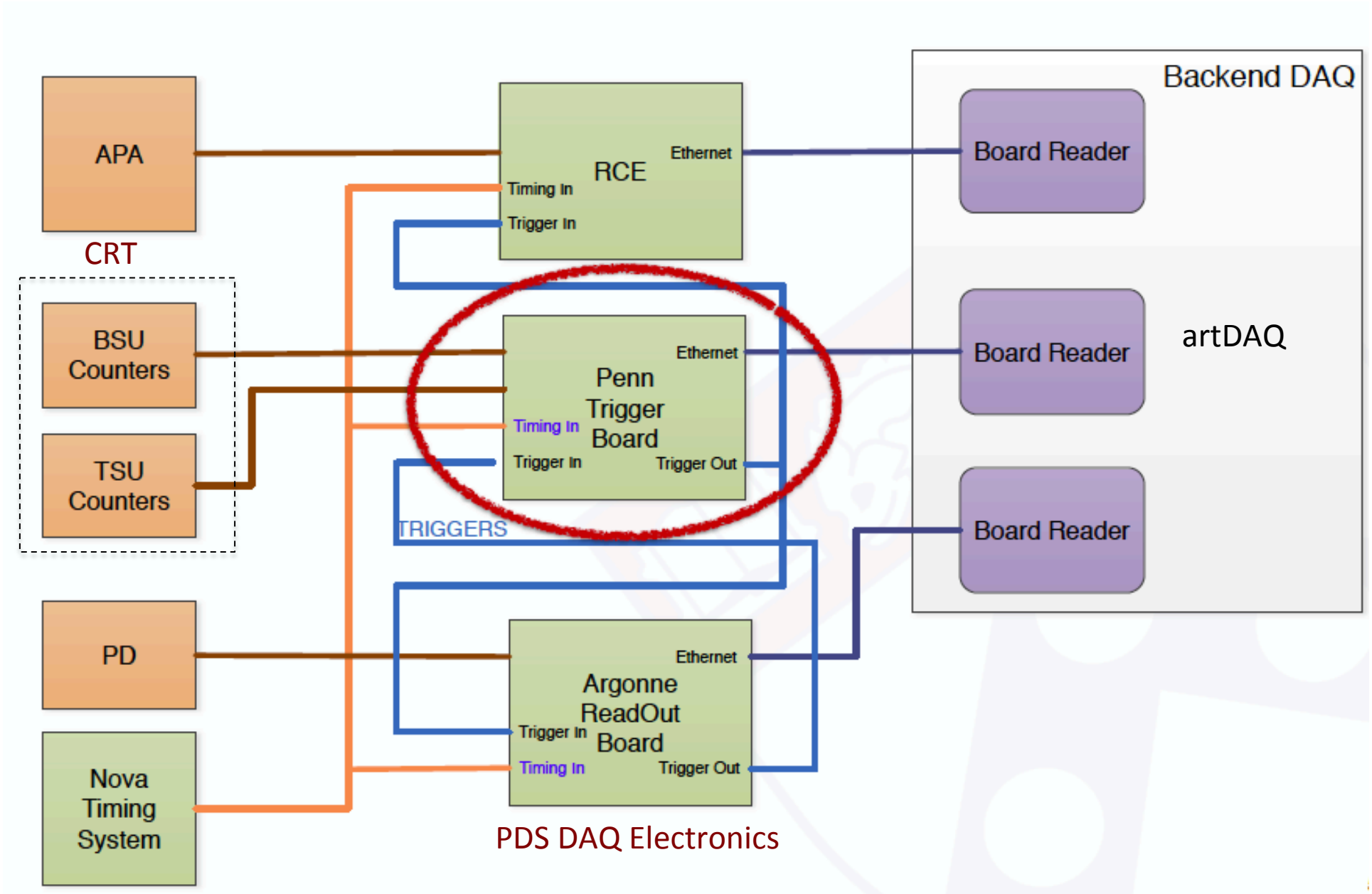
- Receive sub-system triggers and generate global triggers based on an artDAQ-configurable mask, or more sophisticated algorithms if desired
- Time-stamp global triggers, keep event count, provide artDAQ-compatible header information with trigger type, error conditions
- Provide internally generated triggers (random triggers, etc.)
- Act as both a master for some calibrations and a slave to others

Penn Trigger Board

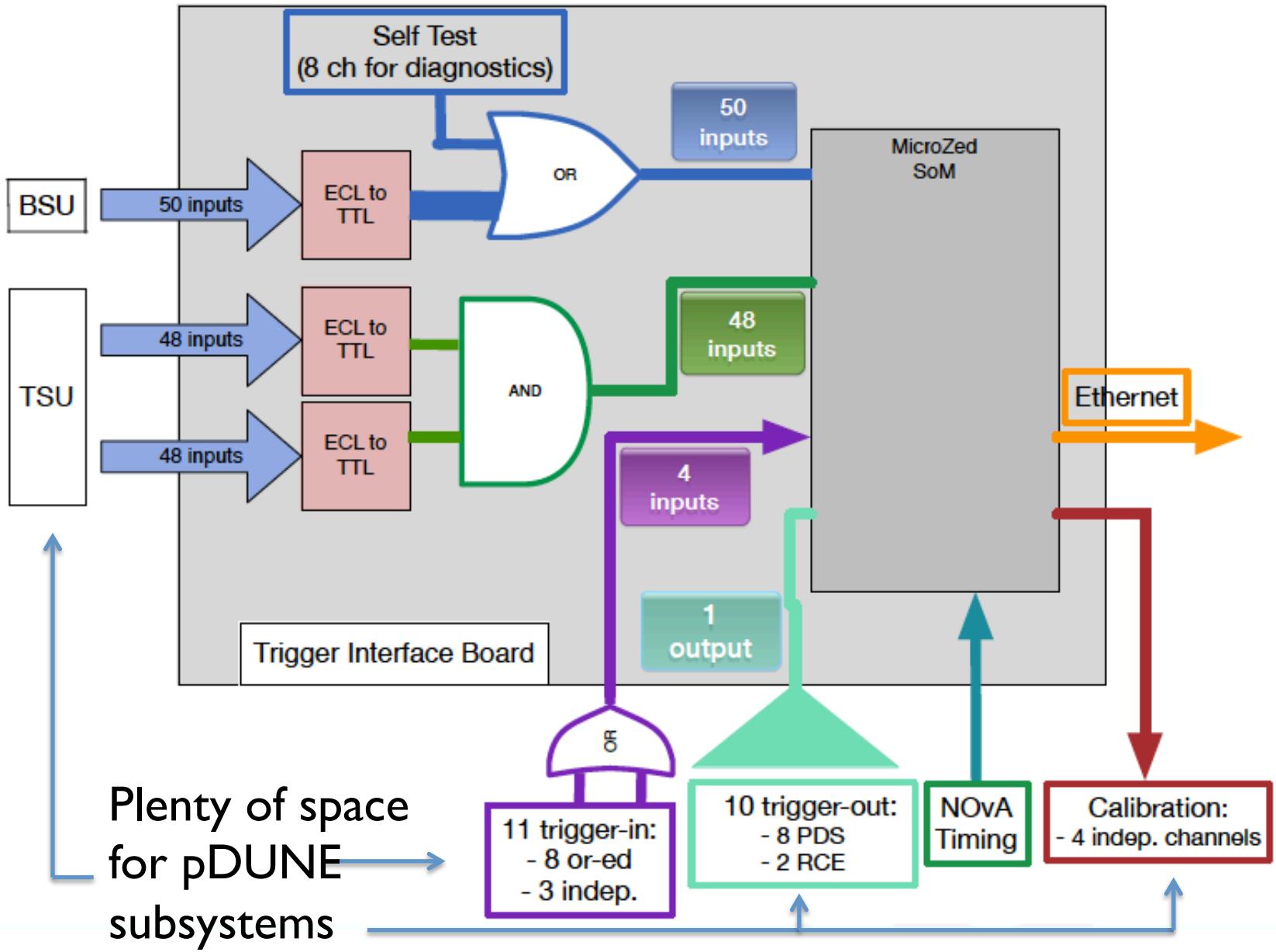
But also:

- Act as front-end *readout* for 35 t CRT, receiving and combining (~100 chans) trigger primitives in arbitrary logical combinations
- Stream all counter information (time of each “hit”) on to central DAQ for later off-line triggering if desired

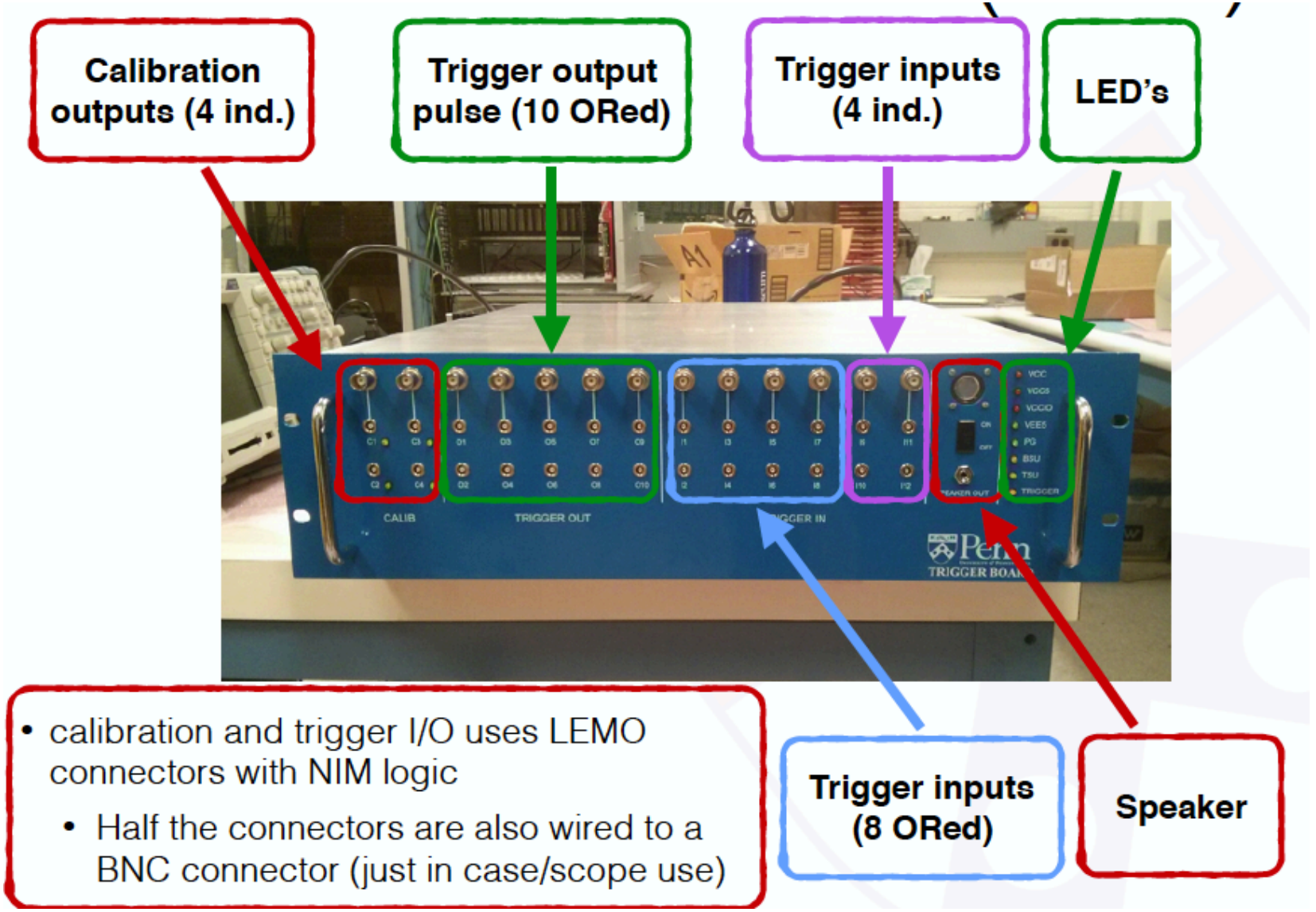
High-Level Overview for 35 t Operations



Lower-Level Block Diagram

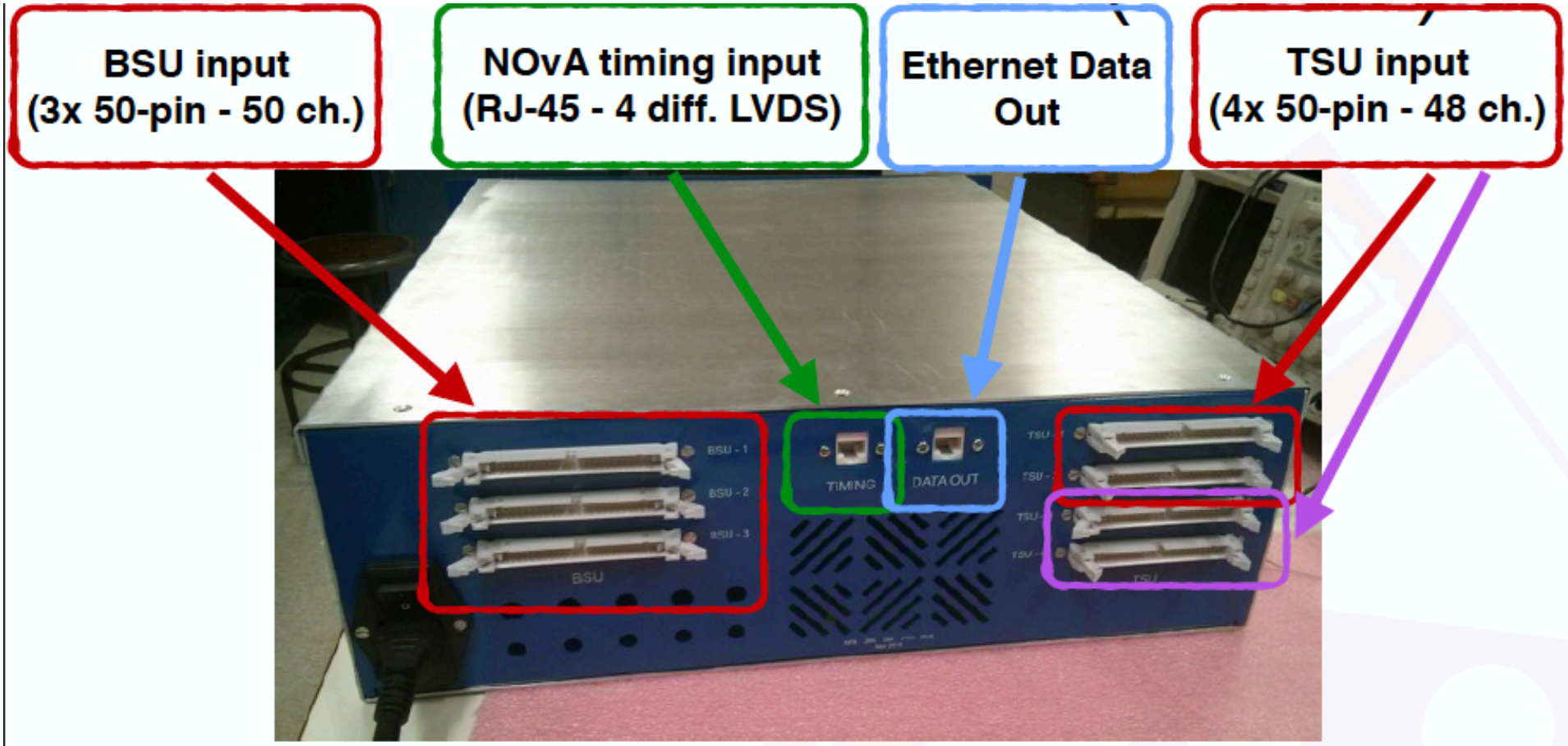


Physical Interface View (Front)



- calibration and trigger I/O uses LEMO connectors with NIM logic
  - Half the connectors are also wired to a BNC connector (just in case/scope use)

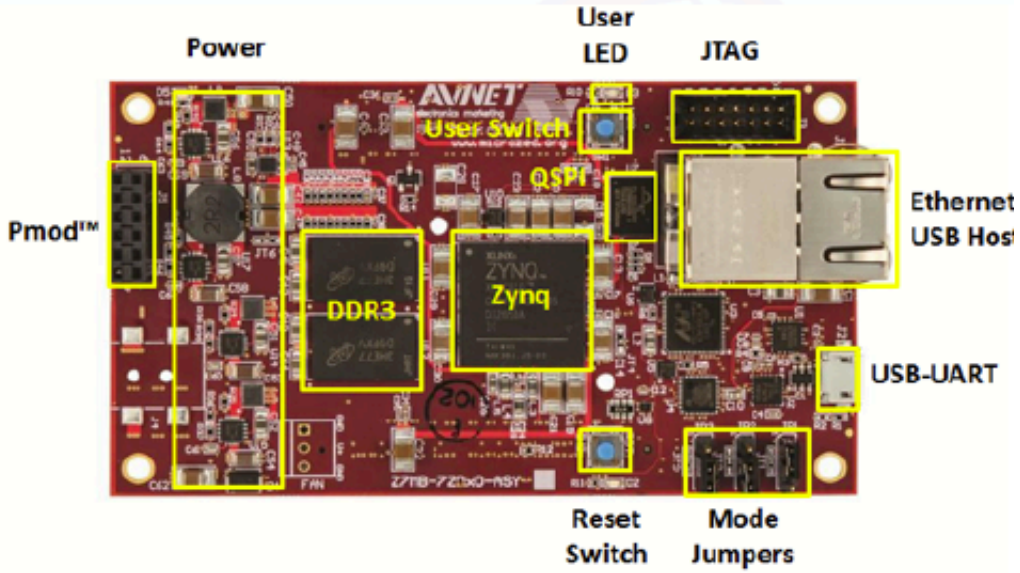
Physical Interface View (Back)



- Inputs in differential ECL
  - The TSU's are ANDed in pairs on the hardware

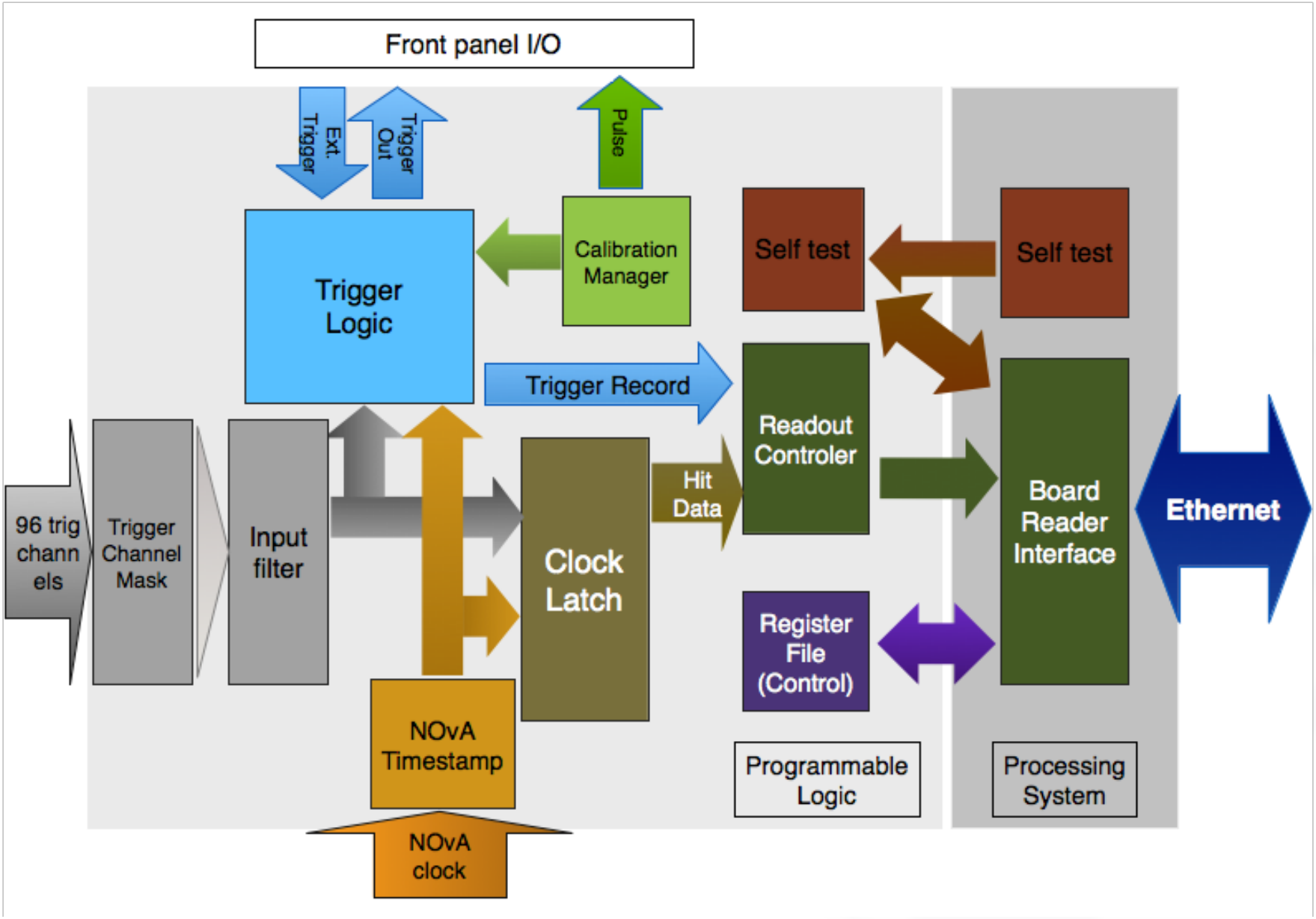
Logical Hardware (microZED)

- Xillinx Zynq-7000 SoC
  - PTB uses Zynq-7Z020
- 1 GB DDR3 RAM
- Gigabit Ethernet
- 115 I/O ports
- 33.33 MHz oscillator



The rest of the PTB is essentially the physical interface to the microZED. Both firmware and software (via Linux) can be used to generate triggers

Existing Firmware Block Diagram



Using PTB for protoDUNE

Inputs:

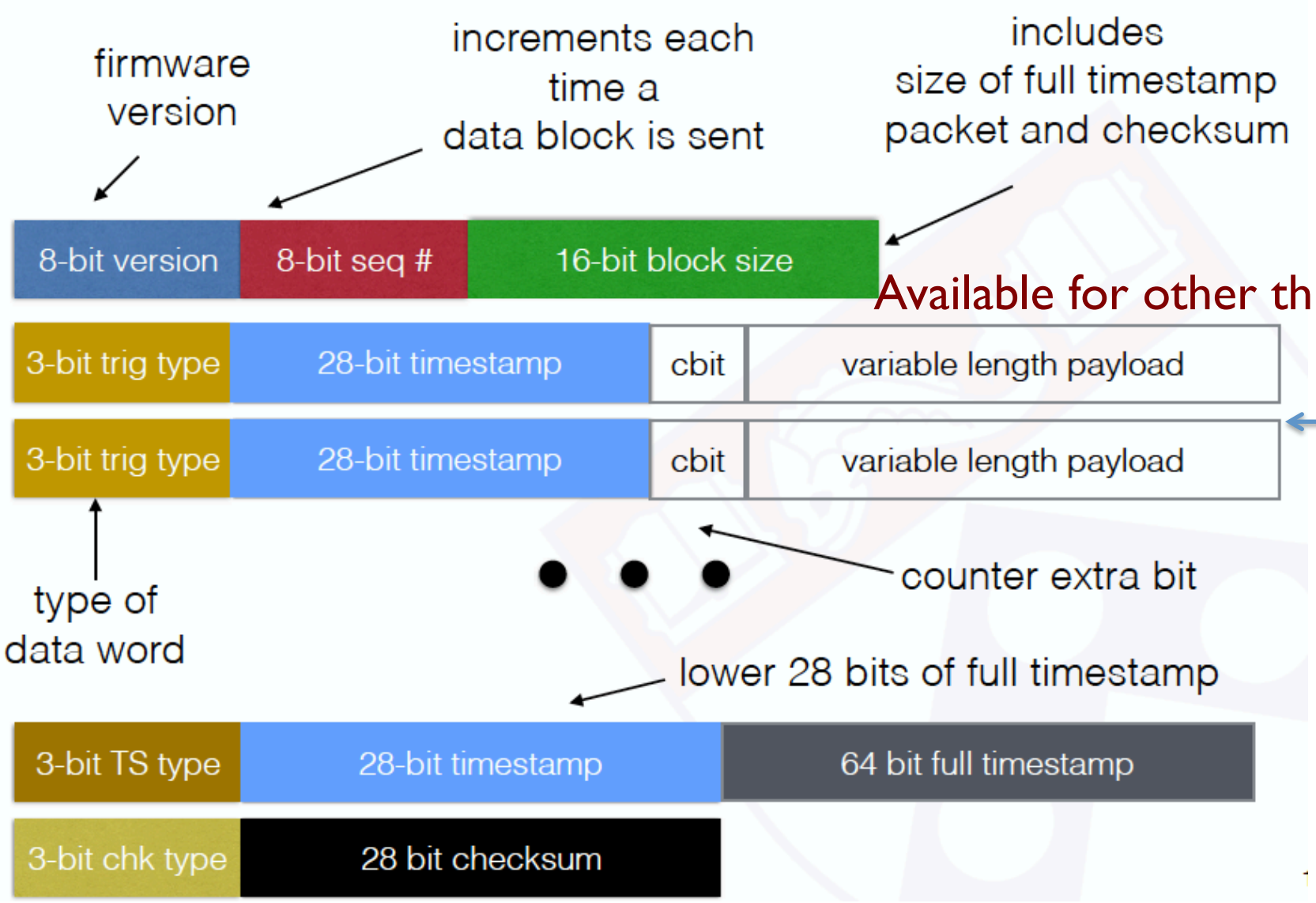
- PDS provides signal or signals from SSPs
- ~~Laser provides its own trigger, sends a copy to PTB~~
- CRT provides output signals (but does not require a trigger)
- Accelerator provides some number of outputs from local NIM logic
- No independent trigger in from TPC (it is slow)
- Timing system provides a clock and a SYNC

Using PTB for protoDUNE

Outputs:

- Global trigger signal or signals from external systems to subsystems
  - Could distribute multiple bits in a trigger word
- "Random" (zero bias) trigger or any other internally-generated signal
- Calibration pulses for front-end electronics or any other subsystems
- artDAQ data fragments (next slide)

Existing Format



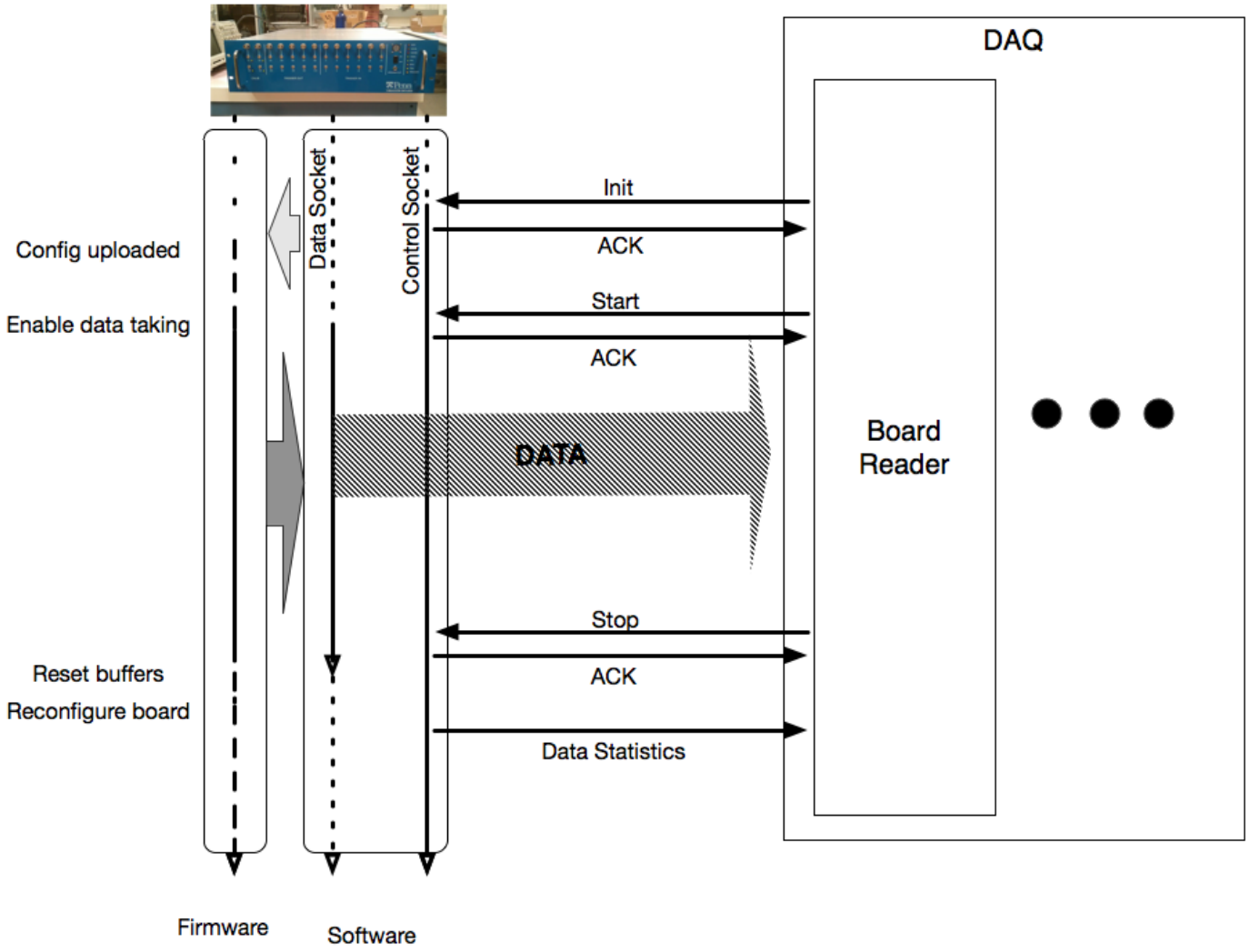
Demands of 35 t counter data far exceed anything for protoDUNE

Using PTB for protoDUNE

Configuration:

- XML configuration file
- FHICL input file used by board reader
  - Translates into XML file sent to PTB
- 2 types of blocks:
  - configuration
  - command
    - start run, stop run, hard reset, soft reset

Using PTB for protoDUNE



Using PTB for protoDUNE

Needed/Desired Changes:

- Firmware updated to use 100 counter inputs as trigger signals
- Interface with new timing system
  - Likely much simpler than NOvA system
- Any new software triggering schemes
- Better physical interface for protoDUNE signals
  - Would like to use simpler connector scheme
  - Change ECL input logic for counter inputs to configurable signal logic (NIM, LVCMOS, ECL…)
- If we stick with old interface, need to make small mods to front-end of the PTB

Total cost to design & fab a new board ~ $1000
Cost of a new box ~$500
Time for new design+fabrication ~2 months